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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/670,797	09/26/2000	William A. Kleinhans	1191	4731

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EXAMINER

VILLECCO, JOHN M

ART UNIT	PAPER NUMBER
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2612

DATE MAILED: 02/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/670,797

Applicant(s)

Examiner

John M. Villecco

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 September 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-3 is/are allowed.
- 6) ☒ Claim(s) 4, 6-9 and 11-20 is/are rejected.
- 7) ☒ Claim(s) 5 and 10 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 16 September 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>9/15/04</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

1. Applicant has amended the claims to more specifically distinguish the timing of the invention over the prior art. More specifically, applicant has added the term “thereafter” in each of the independent claims to specify the order in which the accessing of rows is achieved.

2. Regarding claims 1 and 11, the amendment appears to overcome the prior art of record. However, as for claims 4, 8, 14, and 18, it is the opinion of the examiner that the amendment does not overcome the prior art. Each of claims 4, 8, 14, and 18, merely discloses that row N of the image sensor is accessed a second time. A first way of interpreting this limitation is that, since the imager of Guidash would inherently capture more than one image, row N would be accessed a second time (after accessing row N+1 as stated in the claims) in the next image taken. Therefore, the examiner believes that Guidash (along with many other references) can still be read on the claims 4, 8, 14, and 18, and thus the rejection of the claims will be maintained.

3. Regarding claims 11, 14, and 18, applicant includes the limitation of the scan controller thereafter accesses the first row of the array a second time. A second way of interpreting this limitation is as follows. The phrase “thereafter” in each of claims 11, 14, and 18 is sufficiently vague enough that if any one of the previous actions happen before the scan controller accesses the first row a second time, the limitation is met. Therefore, with reference to claims 11, 14, and 18, Guidash teaches that the first row of the array is accessed a first time, before the first row of the array is accessed a second time. Therefore, the limitation is met. In other words, the addition

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of the word “thereafter” does not specify what step should be performed before the first row is accessed a second time.

4. Therefore, the rejections of claims 11, 14, and 18 from the previous office action will be repeated.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. **Claims 4 and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by**

Guidash (U.S. Patent No. 6,218,656).

7. Regarding **claim 4**, Guidash discloses an active pixel sensor arrangement with shared reset signal and row select lines. More specifically, Guidash discloses a plurality of pixel sensors arranged in an array of rows and columns (col. 3, lines 3). Each row of the array has an access line shared with a reset line of a previous row to form a shared access/reset line which simultaneously access the current row and reset the previous row. The array of pixels includes per column signal processing. This signal processing is identified as correlated double sampling (col. 3, lines 4-13). A reset signal is pulsed and a sample of the reset signal is stored in capacitor, Cr. Then a pixel signal is read out and stored in capacitor, Cs. Accessing the row in order to get a pixel signal is interpreted to be the first time. Then the system selects the next row (N+1) to

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sample. See column 3, line 45 to column 4, line 30 and Figure 2. Inherently, row N will be accessed again in order to obtain a second image. This is interpreted to be the second time.

8. As for *claim 14*, Guidash discloses an active pixel sensor arrangement with shared reset signal and row select lines. More specifically, Guidash discloses a plurality of pixel sensors arranged in an array of rows and columns (col. 3, lines 3). Each row of the array has an access line shared with a reset line of a previous row to form a shared access/reset line which simultaneously access the current row and reset the previous row. The array of pixels includes per column signal processing. This signal processing is identified as correlated double sampling (col. 3, lines 4-13). A reset signal is pulsed and a sample of the reset signal is stored in capacitor, Cr. Then a pixel signal is read out and stored in capacitor, Cs. Then the system selects the next row (N+1) to sample. See column 3, line 45 to column 4, line 30 and Figure 2. Inherently the lines and would be operated by a driver and the driver operated by a scan controller to implement proper timing. As mentioned previously, the phrase “thereafter” is sufficiently vague enough that if any one of the previous actions happen before the scan controller accesses the first row a second time, the limitation is met. Therefore, Guidash teaches that the first row of the array is accessed a first time, before the first row of the array is accessed a second time.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10. **Claims 6-9 and 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Guidash (U.S. Patent No. 6,218,656) in view of Panicacci (U.S. Patent No. 6,529,242).**

11. Regarding *claim 6*, as mentioned above in the discussion of claim 4, Guidash discloses all of the limitations of the parent claim. However, Guidash fails to specifically disclose accessing an $N+1+M$ row of the array to set an image exposure time of the semiconductor imaging chip. Panicacci, on the other hand discloses that it is well known in the art to access rows before reading them out in order to begin the integration process (i.e. set exposure time). Panicacci discloses the use of two shutter pulses. The first shutter pulse begins the integration period by releasing the pixels from reset (col. 2, lines 55-56). As shown in Figure 4, as each row is released from reset a previous row is read out. See column 3, lines 1-35. This method serves an efficient way to establish an exposure time in an APS sensor. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to access a third row ahead of the other rows to begin an integration process so that an efficient exposure method is implemented in Guidash.

12. With regard to *claim 7*, Panicacci discloses in Figure 4, that as the first pointer releases the row from reset, a different row is read out.

13. As for *claim 8*, Guidash discloses an active pixel sensor arrangement with shared reset signal and row select lines. More specifically, Guidash discloses a plurality of pixel sensors arranged in an array of rows and columns (col. 3, lines 3). Each row of the array has an access line shared with a reset line of a previous row to form a shared access/reset line which simultaneously access the current row and reset the previous row. The array of pixels includes per column signal processing. This signal processing is identified as correlated double sampling

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(col. 3, lines 4-13). A reset signal is pulsed and a sample of the reset signal is stored in capacitor, Cr. Then a pixel signal is read out and stored in capacitor, Cs. Accessing the row in order to get a pixel signal is interpreted to be the first time. Then the system selects the next row (N+1) to sample. See column 3, line 45 to column 4, line 30 and Figure 2. Inherently, row N will be accessed again in order to obtain a second image. This is interpreted to be the second time.

Guidash, however, fails to specifically disclose accessing an N+1+M row and setting the image exposure time of the semiconductor imaging chip. Panicacci, on the other hand discloses that it is well known in the art to access rows before reading them out in order to begin the integration process (i.e. set exposure time). Panicacci discloses the use of two shutter pulses. The first shutter pulse begins the integration period by releasing the pixels from reset (col. 2, lines 55-56). As shown in Figure 4, as each row is released from reset a previous row is read out. See column 3, lines 1-35. This method serves an efficient way to establish an exposure time in an APS sensor. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to access a third row ahead of the other rows to begin an integration process so that an efficient exposure method is implemented in Guidash.

14. Regarding **claim 9**, Panicacci discloses in Figure 4, that as the first pointer releases the row from reset, a different row is read out.

15. **Claim 16** is considered substantively equivalent to claim 6. Please see the discussion of claim 6 above.

16. **Claim 17** is considered substantively equivalent to claim 7. Please see the discussion of claim 7 above.

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17. *Claim 18* is considered substantively equivalent to claim 8. Please see the discussion of claim 8 above.

18. *Claim 19* is considered substantively equivalent to claim 9. Please see the discussion of claim 9 above.

19. **Claims 11 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Guidash (U.S. Patent No. 6,218,656, hereinafter referred to as Guidash '656) in view of Guidash (U.S. Patent No. 6,587,146, hereinafter referred to as Guidash '146).**

20. With regard to *claim 11*, Guidash '656 discloses an active pixel sensor arrangement with shared reset signal and row select lines. More specifically, Guidash '656 discloses a plurality of pixel sensors arranged in an array of rows and columns (col. 3, lines 3). Each row of the array has an access line shared with a reset line of a previous row to form a shared access/reset line which simultaneously access the current row and reset the previous row. The array of pixels includes per column signal processing. This signal processing is identified as correlated double sampling (col. 3, lines 4-13). A reset signal is pulsed and a sample of the reset signal is stored in capacitor, Cr. Then a pixel signal is read out and stored in capacitor, Cs. Then the system selects the next row (N+1) to sample. See column 3, line 45 to column 4, line 30 and Figure 2. Inherently the lines and would be operated by a driver and the driver operated by a scan controller to implement proper timing. As mentioned previously, the phrase "thereafter" is sufficiently vague enough that if any one of the previous actions happen before the scan controller accesses the first row a second time, the limitation is met. Therefore, Guidash teaches

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that the first row of the array is accessed a first time, before the first row of the array is accessed a second time.

Guidash '656, however, fails to specifically disclose canceling the internal offset voltage of the active pixel sensor. Guidash '146, on the other hand, discloses that it is well known in the art to sample an active pixel sensor a plurality of times to cancel an offset voltage of the pixel sensor. In column 4, lines 60-67, Guidash '146 teaches that the process operates to cancel the pixel source follower offset voltage. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to also cancel the offset voltage in Guidash '656 in order to form a better image.

21. Regarding **claim 15**, as mentioned above in the discussion of claim 14, Guidash '656 discloses all of the limitations of the parent claim. However, Guidash '656 fails to specifically disclose canceling an internal offset voltage. Guidash '146, on the other hand, discloses that it is well known in the art to sample an active pixel sensor a plurality of times to cancel an offset voltage of the pixel sensor. In column 4, lines 49-67, Guidash '146 teaches that the process operates to cancel the pixel source follower offset voltage by storing first and second pixel samples in capacitors C_r and C_s and subtracting the difference using the difference amplifier (32). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to also cancel the offset voltage in Guidash '656 in order to form a higher quality image.

22. **Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Guidash (U.S. Patent No. 6,218,656, hereinafter referred to as Guidash '656) in view of**

Guidash (U.S. Patent No. 6,587,146, hereinafter referred to as Guidash '146) and further in view of Panicacci (U.S. Patent No. 6,529,242).

23. Regarding *claim 12*, as mentioned above in the discussion of claim 11, both Guidash '656 and Guidash '146 disclose all of the limitations of the parent claim. However, neither of the aforementioned references discloses accessing a row ahead of the previous rows in order to set an image exposure time, nor even how an exposure time is even set. Panicacci, on the other hand discloses that it is well known in the art to access rows before reading them out in order to begin the integration process (i.e. set exposure time). Panicacci discloses the use of two shutter pulses. The first shutter pulse begins the integration period by releasing the pixels from reset (col. 2, lines 55-56). As shown in Figure 4, as each row is released from reset a previous row is read out. See column 3, lines 1-35. This method serves an efficient way to establish an exposure time in an APS sensor. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to access a third row ahead of the other rows to begin an integration process so that an efficient exposure method is implemented in Guidash.

24. As for *claim 13*, Panicacci discloses in Figure 4, that as the first pointer releases the row from reset, a different row is read out.

25. **Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Guidash (U.S. Patent No. 6,218,656, hereinafter referred to as Guidash '656) in view of Panicacci (U.S. Patent No. 6,529,242) and further in view of Guidash (U.S. Patent No. 6,587,146, hereinafter referred to as Guidash '146).**

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26. Regarding *claim 20*, as mentioned above in the discussion of claim 18, both Guidash '656 and Panicacci disclose all of the limitations of the parent claim. However, neither of the aforementioned references discloses canceling an internal offset voltage. Guidash '146, on the other hand, discloses that it is well known in the art to sample an active pixel sensor a plurality of times to cancel an offset voltage of the pixel sensor. In column 4, lines 49-67, Guidash '146 teaches that the process operates to cancel the pixel source follower offset voltage by storing first and second pixel samples in capacitors Cr and Cs and subtracting the difference using the difference amplifier (32). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to also cancel the offset voltage in Guidash '656 in order to form a higher quality image.

Allowable Subject Matter

27. Claims 5 and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding *claims 5 and 10*, the primary reason for indication of allowable subject matter is that the prior art fails to teach or reasonably suggest that the method used for canceling the internal offset voltage at the output of a pixel sensor includes storing a first sample of the pixel sensor in row N during the first time, storing a second sample of the pixel sensor in row N during the second time, and subtracting the second sample from the first sample to form a corrected output.

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28. Claims 1-3 are allowed.

29. The following is an examiner's statement of reasons for allowance:

Regarding claim 1, the primary reason allowance is that the prior art fails to teach or reasonably suggest a method for canceling the internal offset voltage of a pixel including the steps of accessing a first row of the array, storing a first sample of a pixel sensor of the first row, accessing a second row of an array, thereafter accessing the first row a second time to obtain a second sample of the pixel sensor, storing the second sample, subtracting the second sample from the first sample to from a corrected output.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

30. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a):

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

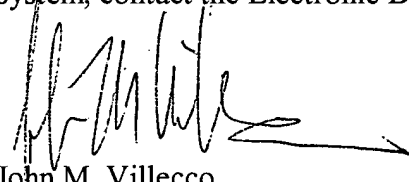
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however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

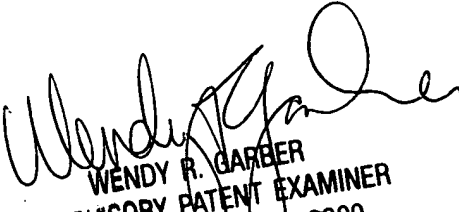
Any inquiry concerning this communication or earlier communications from the examiner should be directed to John M. Villecco whose telephone number is (703) 305-1460 (Crystal City) or (571) 272-7319 (Carlyle). The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy Garber can be reached on (703) 305-4929 (Crystal City) or (571) 272-7308 (Carlyle). The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



John M. Villecco
January 26, 2005



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SUPERVISORY PATENT EXAMINER
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